Journal of Basic and Applied Engineering Research
Print ISSN: 2350-0077; Online ISSN: 2350-0255; Volume 1, Number 12; October-December 2014 pp. 106-109

http://www.krishisanskriti.org/jbaer.html

FPGA Based IIR Filter Design Analysis for Different Orders

Anurag Yadav[1] and Rajesh Mehra[2]

[1]ME Scholar Department of Electronics and Communication Engineering, NITTTR, Sector- 26, Chandigarh, , India
[2]Department of Electronics and Communication Engineering, NITTTR, Sector- 26, Chandigarh, India
E-mail: [1]anuraglko2014@gmail.com

Abstract: Filter is the most important element in digital signal processing. Infinite Impulse Response (IIR) filter is a digital filter. Based on FPGA different order of low pass IIR filters are designed. To design the different order of IIR filters VHDL is used. The VHDL codes have been synthesized with the Xilinx integrated software environment ISE. After synthesis compare the area utilization of different order of low pass IIR filter and then find the time delay for different order low pass IIR filter. Time delay gives the information of speed.IIR filter which has minimum time delay gives better response than others. Area utilization and time delay are two important factors to design any filter. Order of any filter also selects on the basis of area utilization and time delay.

Keywords: *IIR filter, FPGA, VHDL*

1. INTRODUCTION

Digital signal processing is an important component of digital communication systems and filters are the most common elements in digital signal processing. In this paper distributed arithmetic (DA) based IIR filter approach used that reduces the number of tabs at the input for filter response.[1] The function of a filter is to eliminate unwanted portion in signal and to resolve signals into their frequency components. Filter has two types analog and digital. In analog filters input and output both are continuous time signals but in digital filters input and output both are discrete time signals. Digital filter has two types FIR and IIR filter. Digital filters use a digital processor to perform mathematical calculations on signal's sampled values. One another approach is to use Field Programmable Gate Array (FPGA).[2] Digital filters require analog to digital convertor and digital to analog convertor sections for connecting to the physical analog world. Main advantages of digital filters are that these are insensitive to noise high accuracy and high linearity.

Digital filters are rapidly replacing classic analog filters, which we implemented using RLC components and operation amplifiers. Analog filters were mathematically ordinary differential equations of Laplace transform.[3] Digital filters have better reliability and stability for these reasons digital filters are widely used in communication, automatic control, aerospace, medicine radar and in so many applications. Digital filter are vastly superior in the level of performance.FPGA is specifically designed to meet the requirements of cost effective, high volume consumer electronic applications. FPGA avoid the high initial cost, the lengthy development cycles, and the inherent inflexibility of digital signal processor. FPGA programmability permits design upgrades in the field with no hardware replacement necessary. FPGA have configurable logic block, Input Output block and routing channels in its architecture. Configurational logic blocks contain look up tables LUTS to implement logic and store elements in flip flop. These look up tables and flip-flop arrange in slices.[4]

The important advantage of IIR filter on FIR filter is its implementation efficiency. IIR filters require less number of orders as comparison to meet same specification. FPGA based IIR filter design can reduces the computational complexity because FPGA use distributed arithmetic which reduces the number of tabs for filter response. FPGA provides more logic flexibility and the power consumption is low. FPGA is a semiconductor device containing programmable logic components and programmable interconnects.

2. INFINITE IMPULSE RESPONSE (IIR) FILTER

IIR digital filters are recursive in nature. IIR filter is characterized by the following equation:

$$Y(n) = \sum_{k=0}^{\infty} h(k)x(n-k) \quad (1)$$

$$Y(n) = \sum_{k=0}^{N} b_k x(n-k) - \sum_{k=1}^{M} a_k y(n-k) \quad (2)$$

Where h(k) is the impulse response of the filter . a_k and b_k are the coefficients of the filter and x(n) and y(n) are the input and output to the filter .The output sample ,y(n) is a function past outputs, y(n-k), as well as present and past input samples x(n-k) that is the IIR filter is a feedback system. IIR filter is

also known as the recursive filter. The transfer function for the IIR filter is given by

$$H(Z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2} + \ldots\ldots\ldots + b_N z^{-N}}{1 + a_1 z^{-1} + a_2 z^{-2} + \ldots\ldots\ldots + a_M z^{-M}} \quad (3)$$

$$H(Z) = \frac{\sum_{k=0}^{N} b_k z^{-k}}{1 + \sum_{k=1}^{M} a_k z^{-k}} \quad (4)$$

It is very important to find the suitable value of coefficients a_k and b_k such that the magnitude response and phase response acts in a desired manner. [5] Code can find out with the help of Matlab and design the IIR filter with Xilinx ISE tool. These coefficients are get stored in the ROM as LUT memory for the multiplication with data samples stored in the RAM.[6]

IIR filter is also known as the recursive filter. A recursive means feedback connection exists from output to the input. For the realization of IIR filter past, present and future samples of input and past values of output should known for the realization of IIR. The three major factors which is necessary for the realization of filter. These are computational complexity, memory requirements, and finite world length effects in the computations. There are different type of realization Direct form structure, parallel form structure and cascade form structure. Direct form structure has two types Direct form -I structure and Direct form -II structure .Direct form -II structure used in this paper. All the structure has different type of designing. With proper selection of structure computational complexity will reduce.

In this paper Butterworth low pass IIR filter is being developed in VHDL platform for different orders and compare their performance in terms of area utilization and time delay.[7] Matlab gives the opportunity to standardize and convert our coefficients in fixed point and also to test the effect optimization of IIR filter through the different settings available and reduce the errors caused by quantification of IIR filters and it also increase the performance of IIR filter.[8] IIR filter require lesser no of arithmetic operation and these have lower computational complexity and smaller memory requirements.

3. IIR DESIGN SIMULATION

Magnitude response, phase response, impulse response and step response of Butterworth low pass IIR filter obtained in Matlab with sampling frequency 48000Hz and cut-off frequency 10800Hz. The filter coefficients for 16 order, 24order and 32order low pass IIR filters were taken and stored in look-up tables and memory for synthesis in VHDL. These responses for 16 order low pass IIR filter are shown below. Fig. 1 shows the magnitude response of 16 order low pass IIR .It shows the variation of magnitude (db) with respect to frequency. Fig. 2 shows the phase response (radian) of 16 order low pass IIR filter. It shows the variation of phase with respect to frequency. Fig. 3 shows the Impulse response of 16 order low pass IIR filter. It shows the variation of amplitude with respect to time. Fig. 4 shows the step response of 16 order low pass IIR filter. It shows the variation of amplitude with respect to time.

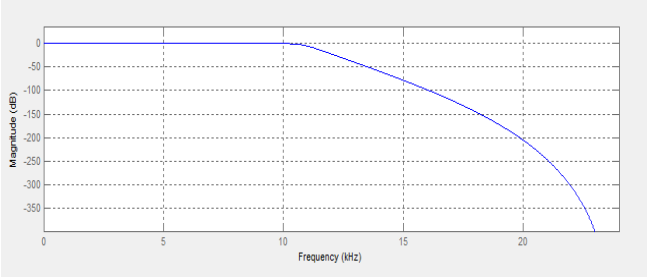

Fig. 1. Magnitude response of 16 order IIR Filter

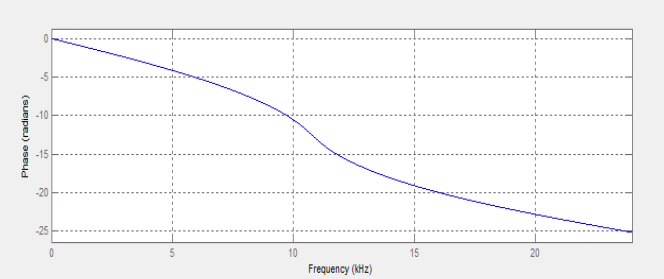

Fig. 2. Phase response of 16 order IIR Filter

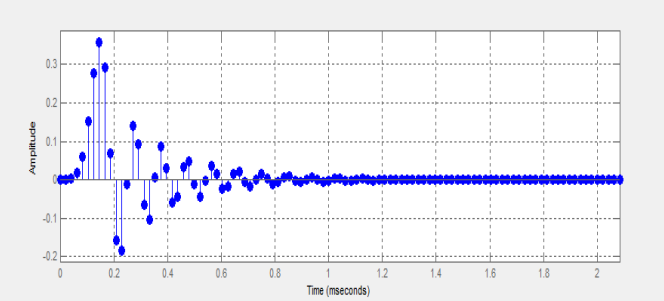

Fig. 3. Impulse response of 16 order IIR Filter

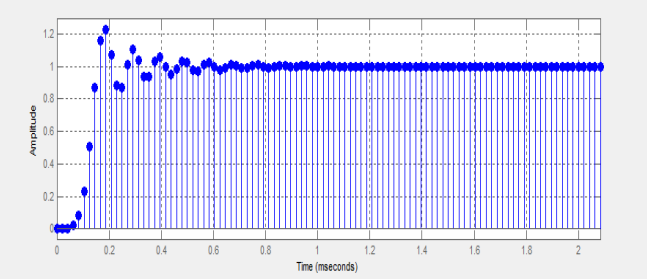

Fig. 4. Step response of 16 order IIR Filter

4. IIR DESIGN SYNTHESIS

Synthesis of low pass IIR filter is based on the VHDL. VHDL code has been synthesized with the Xilinx ISE tool. FPGA Device XC3S1500 used for design of IIR filters. FPGA have Configurational logic blocks contain look up tables LUTS to implement logic and store elements in flip flop. ISE tool can find area utilization for different orders of IIR filters and then compare the area utilization for filter order 16, order 24 and order 32. Comparison of area used is shown in Table1 below in terms of utilization of number of slices, number of slice flip flop, number of 4 input LUTs, number of bonded IOBs, number of multiplier, number of general clocks.

Table 1: Comparison area utilization of IIR filters

Device Area Utilization Summary for IIR Filter				
Logic Utilization for Device XC3S1500	Availabl e	Filter Order 16	Filter Order 24	Filter Order 32
		Used	Used	Used
Number of Slices	13312	835	1542	2821
Number Of Slice Flip Flops	26624	287	415	549
Number of 4 input LUTs	26624	1389	2658	5072
Number of bonded IOBs	221	35	35	35
Number of MULT 18 × 18s	32	24	32	32
Number of GCLKs	8	1	1	1

Xilinx used for the analysis of area utilization and time delay. Matlab used to provide the filter specification. Butterworth low pass IIR filter with different order selected from the options of specification. Now, the code generated for this specification which based on VHDL. Xilinx ISE tool used to synthesize this code. Input of the filters are filter_in(15:0), clk, clk_enable, reset and the output of filter is filter_out(15:0). The simulation results are shown in the Fig. 5, Fig. 6 and Fig. 7.Table 2 shows the area utilization of filter order 16, filter order 24 and filter order 32 in percentage. It gives the comparisons of area utilization among different order low pass IIR filters. After comparison 16 order IIR filter found less area utilization for device XCS1500.

Table 2: Comparisons for percentage area utilization

Logic Area Utilization for Device XC3S1500	**Filter Order 16**	**Filter Order 24**	**Filter Order 32**
	Utilizatio n	**Utilizatio n**	**Utilizatio n**
Number of Slices	6%	11%	21%
Number Of Slice Flip Flops	1%	1%	2%
Number of 4 input LUTs	5%	9%	19%
Number of bonded IOBs	15%	15%	15%
Number of MULT18 × 18s	75%	100%	100%
Number of GCLKs	12%	12%	12%

The time delay in different order of IIR filters which are shown in Table3. Time delay for 16 order IIR filter is 224.958ns, time delay for 24 orders IIR filter is 337.849ns and for 32 order IIR filter is 450.725ns. The time delay in 16 order IIR filter order is minimum compare the 24 order and 32 order IIR filter. So, the 16 order IIR filter perform faster than others.

Table 3: Comparison for time delay in IIR filters

Time Delay of different order IIR filters	
Order of IIR filter	**Time Delay**
16	224.958ns
24	337.849ns
32	450.725ns.

Simulation is the execution of IIR filters in the software environment. This is done using the Xilinx ISE tool. A test bench is a program whose purpose to find out the behavior of IIR filters. The test bench is used to simulate IIR filters design by specifying the inputs into system. Xilinx ISE Simulator results of different order IIR filters are shown below.

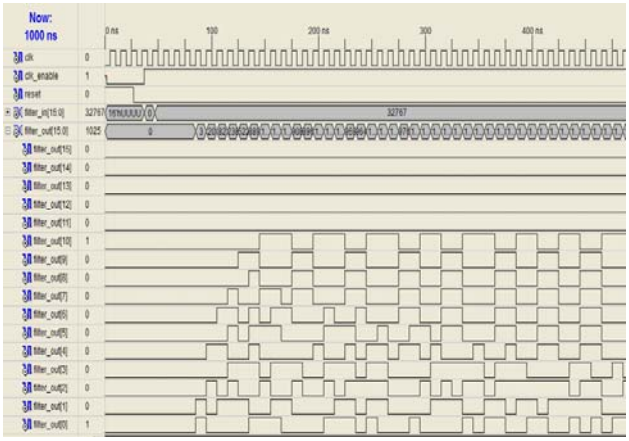

Fig. 5: Xilinx ISE simulation result for 16 order IIR filter

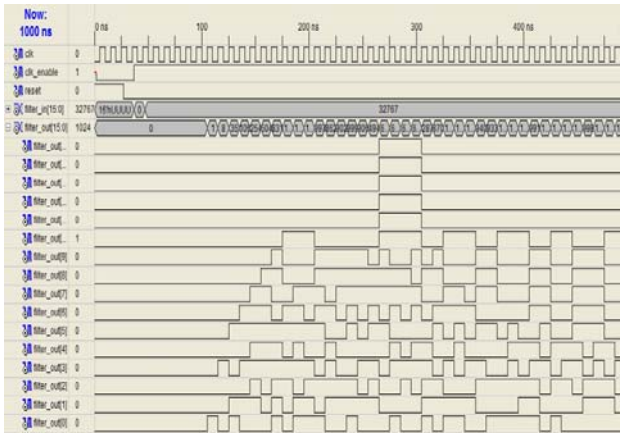

Fig. 6: Xilinx ISE simulation result for 24 order IIR filter

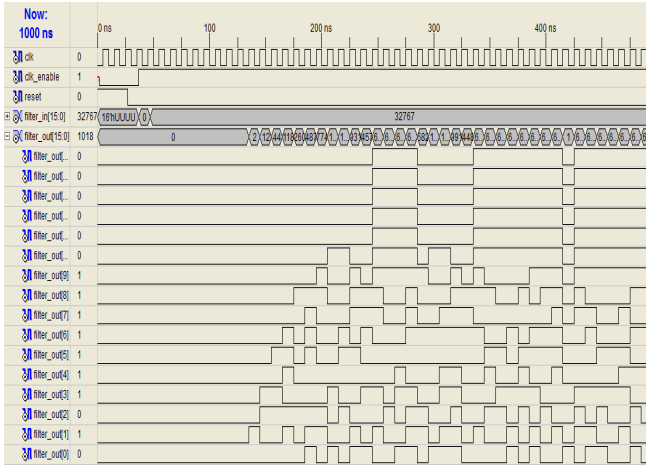

Fig. 7: Xilinx ISE simulation result for 32 order IIR filter.

5. CONCLUSION

In this paper different order of low pass IIR filters are designed which mainly based on FPGA. The VHDL code has been synthesized with the Xilinx ISE tool. Compare the percentage of area utilization of different order IIR filter. The IIR filter with minimum filter order has minimum area utilization. The low order of IIR filter has also minimum time delay. The low order IIR filter has better time response. The low order IIR filter has better speed as well as minimum area utilization. For minimum area consumption and better time response the order of IIR filter should be as minimum as possible.

REFERENCES

[1] Zeynep Kaya, Erol Seke “Direct Generation of Upsampled FIR Filter Response A Simple Extension to Filters with Distributed Arithmetic” 10th International Conference on Digital Technologies, pp110, 2014

[2] Sheikh Md. Rabiul Islam, Robin Sarker, Shumit Saha, A. F. M. Nokib Uddin “Design of a programmable digital IIR filter based on FPGA” IEEE International Conference on Infonnatics, Electronics & Vision, pp716, 2012

[3] Gokulananda Sahu, Kamalakanta Mahapatra “Real Time Implementation of Digital Filter on Control strategy of Dstatcom for Load Compensation under Distorted Utility Condition” IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (Prime Asia), pp166, 2013

[4] Xilinx Spartan-3 FPGA Family Data Sheet DS099 (v3.1) June 27, 2013, pp2

[5] Emmanuel C. Ifeachor , Barrie W. Jervis “Digital Signal Processing A Practical Approach” Pearson Education, Second Edition , pp455, 2004

[6] Santosh Bhalke, Manjula B.M., Dr.Chirag Sharma “FPGA implementation of efficient FIR filter with quantized fixed point coefficients”, pp2, 2013

[7] Ashish Francis, Riboy Cheriyan “Proficient Envelope Shaping Filter for Fading Wireless Channel Estimation” International Conference on Magnetics, Machines & Drives , pp1, 2014

[8] Hadjer Zairi, Malika Kedire-Talha, Sara Benouar, Amine Ait–Amer “Intelligent System for Detecting Cardiac Arrhythmia on FPGA” 5th International Conference on Information and Communication Systems ” , pp4, 2014.